FIG. 1

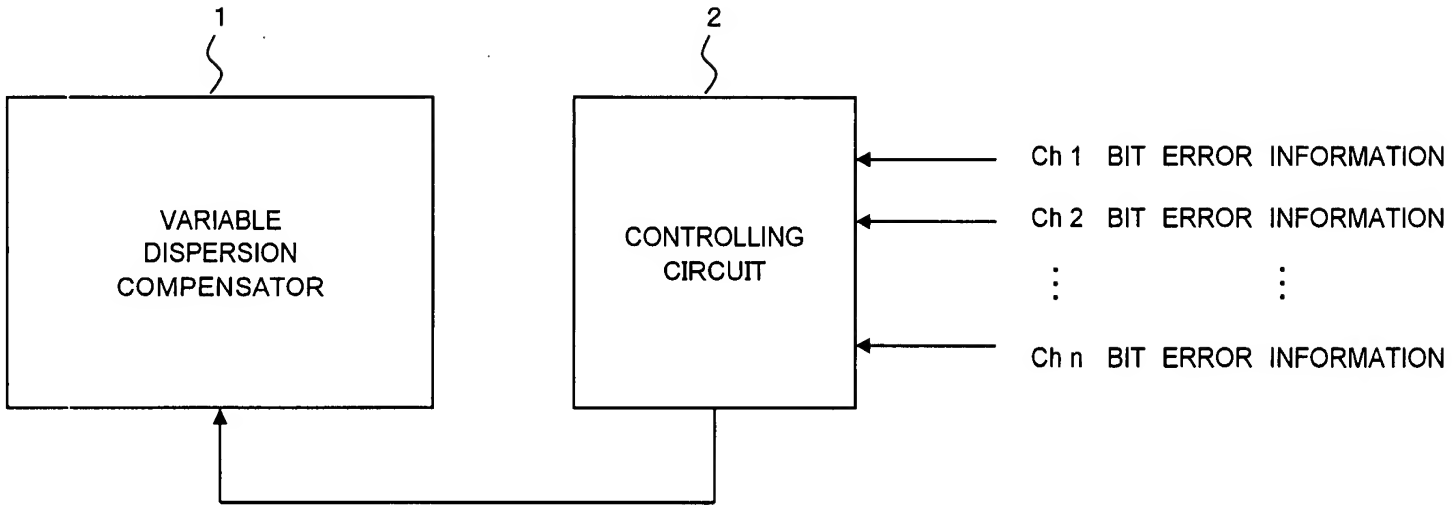

1
2
VARIABLE DISPERSION COMPENSATOR
CONTROLLING CIRCUIT
Ch 1 BIT ERROR INFORMATION
Ch 2 BIT ERROR INFORMATION
Ch n BIT ERROR INFORMATION

FIG. 2

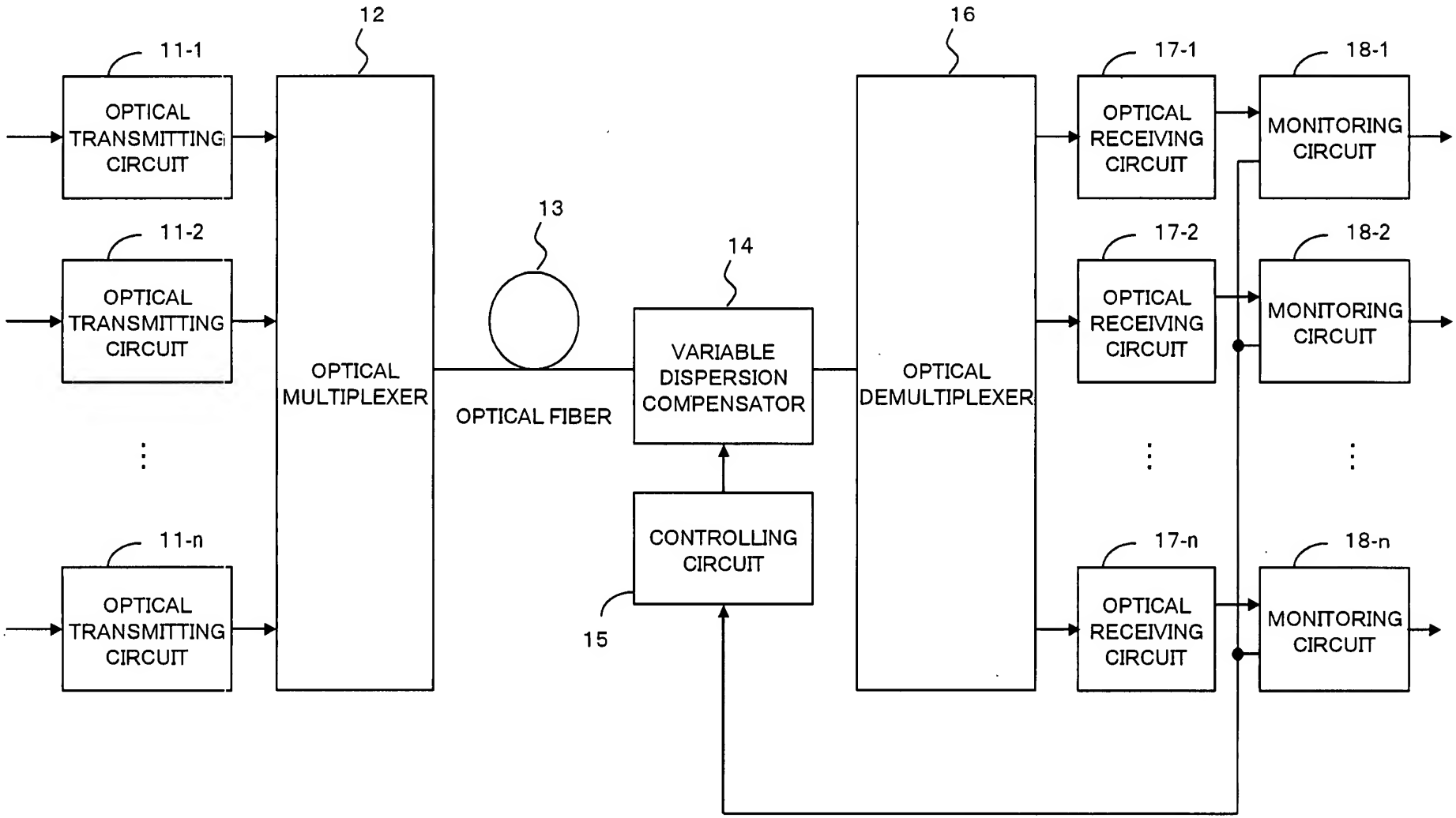

11-1
OPTICAL TRANSMITTING CIRCUIT
11-2
OPTICAL TRANSMITTING CIRCUIT
11-n
OPTICAL TRANSMITTING CIRCUIT
12
OPTICAL MULTIPLEXER
13
OPTICAL FIBER
14
VARIABLE DISPERSION COMPENSATOR
15
CONTROLLING CIRCUIT
16
OPTICAL DEMULTIPLEXER
17-1
OPTICAL RECEIVING CIRCUIT
17-2
OPTICAL RECEIVING CIRCUIT
17-n
OPTICAL RECEIVING CIRCUIT
18-1
MONITORING CIRCUIT
18-2
MONITORING CIRCUIT
18-n
MONITORING CIRCUIT

FIG. 3

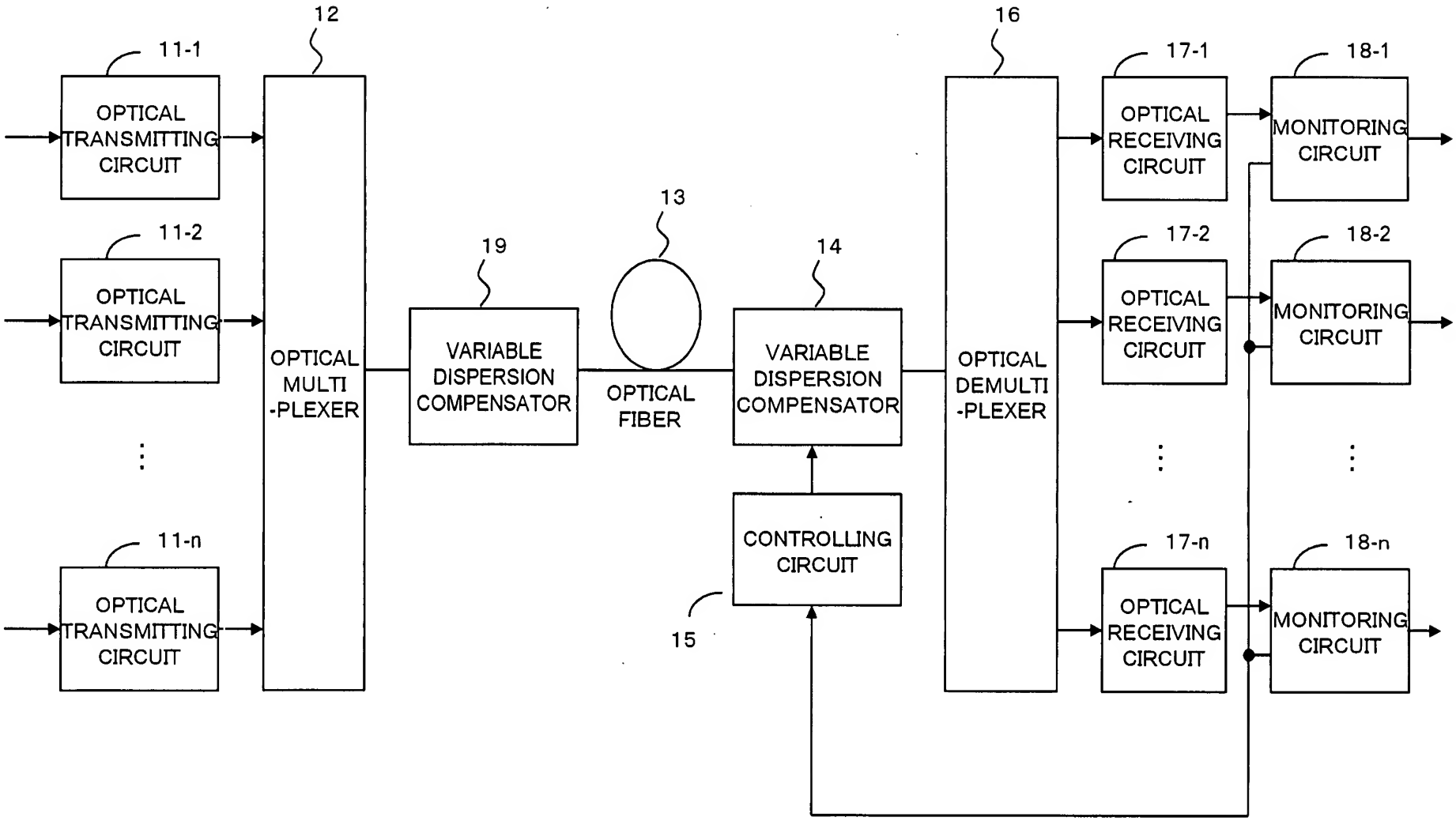

11-1
OPTICAL TRANSMITTING CIRCUIT
11-2
OPTICAL TRANSMITTING CIRCUIT
11-n
OPTICAL TRANSMITTING CIRCUIT
12
OPTICAL MULTI -PLEXER
19
VARIABLE DISPERSION COMPENSATOR
13
OPTICAL FIBER
14
VARIABLE DISPERSION COMPENSATOR
15
CONTROLLING CIRCUIT
16
OPTICAL DEMULTI -PLEXER
17-1
OPTICAL RECEIVING CIRCUIT
17-2
OPTICAL RECEIVING CIRCUIT
17-n
OPTICAL RECEIVING CIRCUIT
18-1
MONITORING CIRCUIT
18-2
MONITORING CIRCUIT
18-n
MONITORING CIRCUIT

FIG. 4

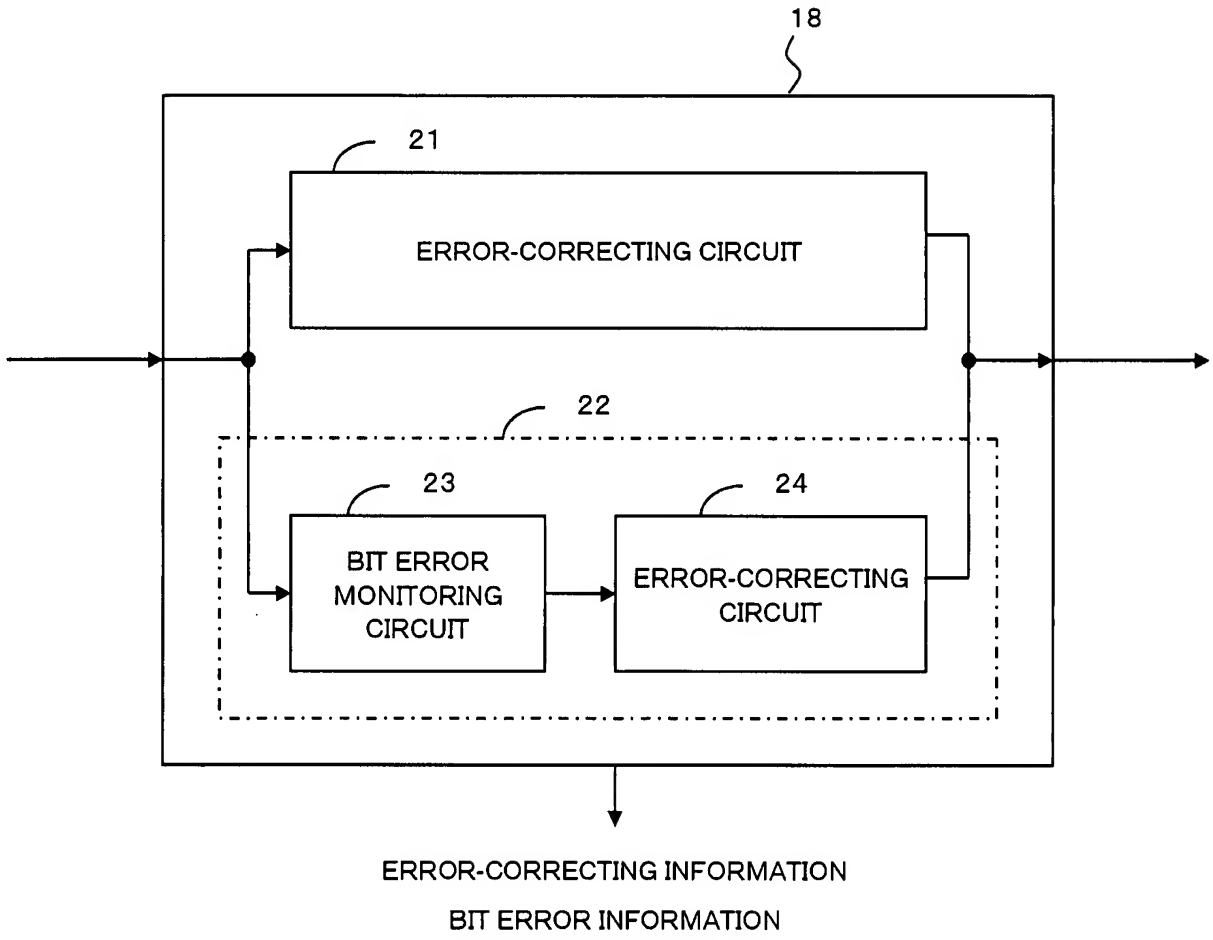

18
21
ERROR-CORRECTING CIRCUIT
22
23
BIT ERROR MONITORING CIRCUIT
24
ERROR-CORRECTING CIRCUIT
ERROR-CORRECTING INFORMATION
BIT ERROR INFORMATION

FIG. 5A

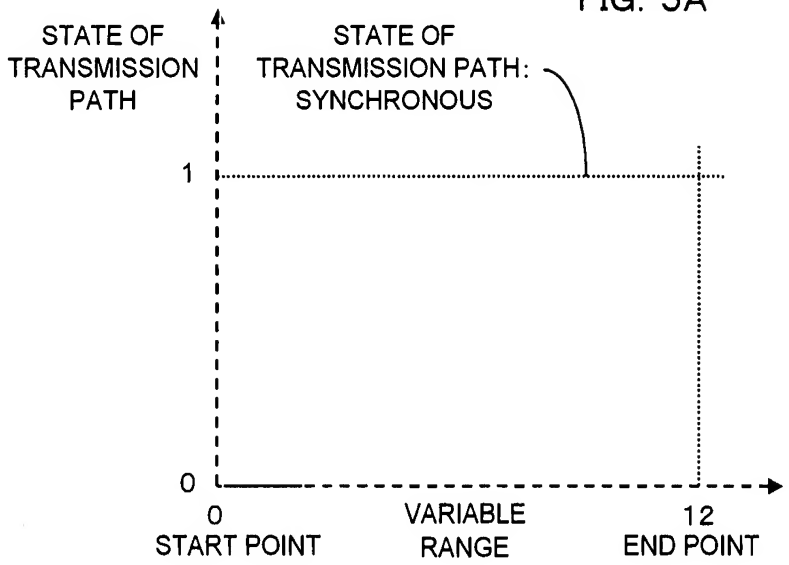



FIG. 5B

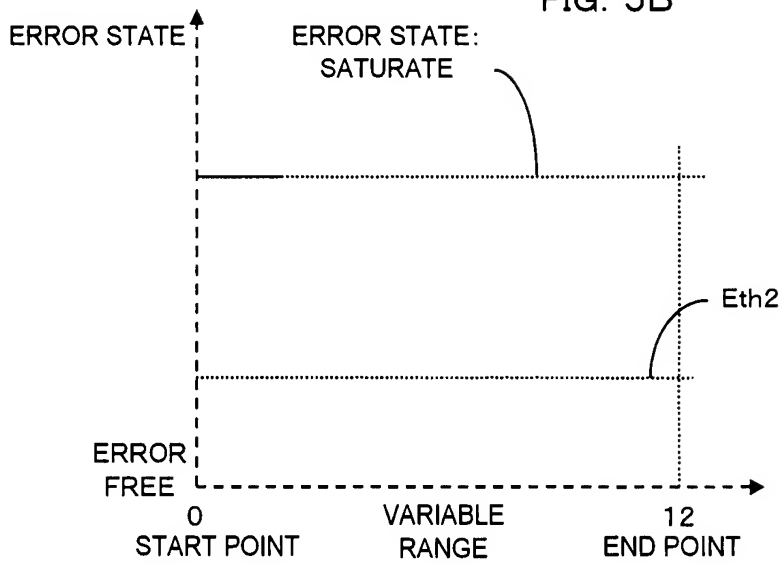



FIG. 5C

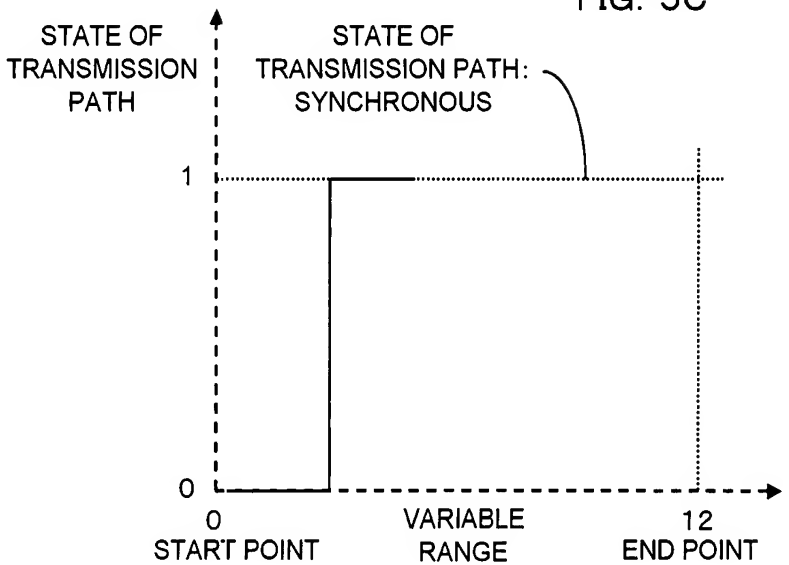



FIG. 5D

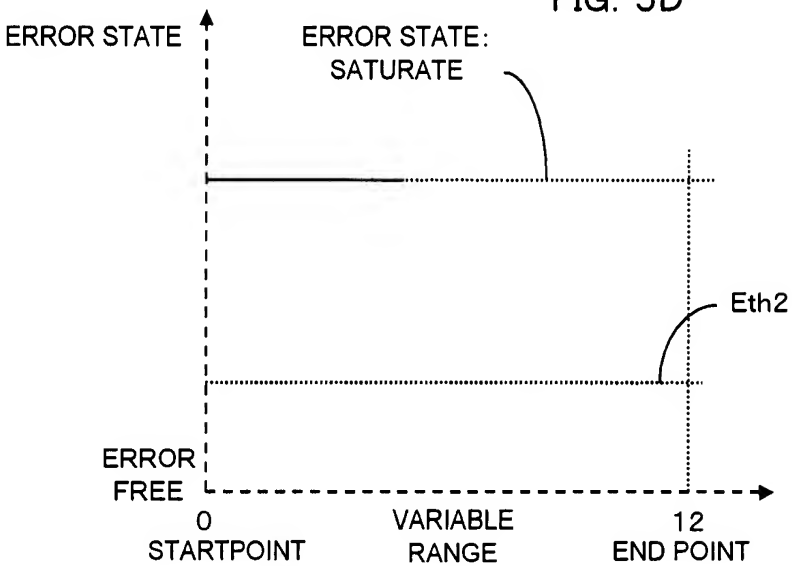


FIG. 6A

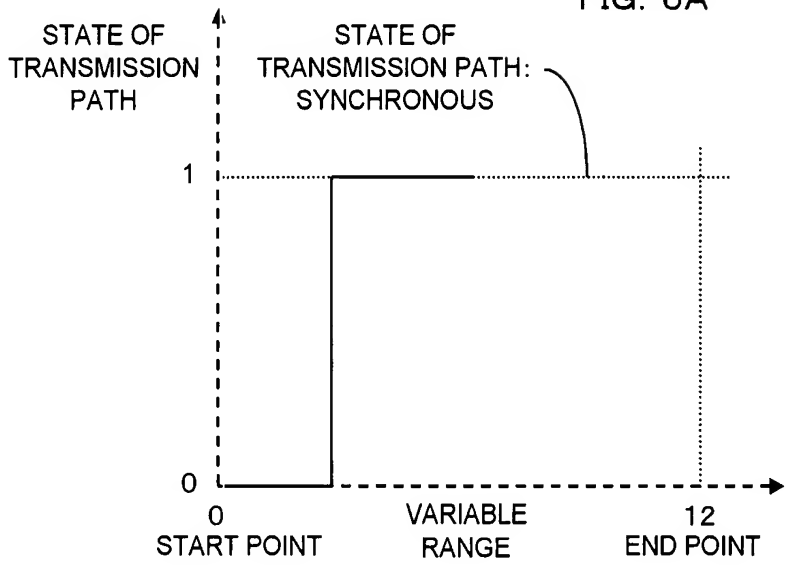



FIG. 6B

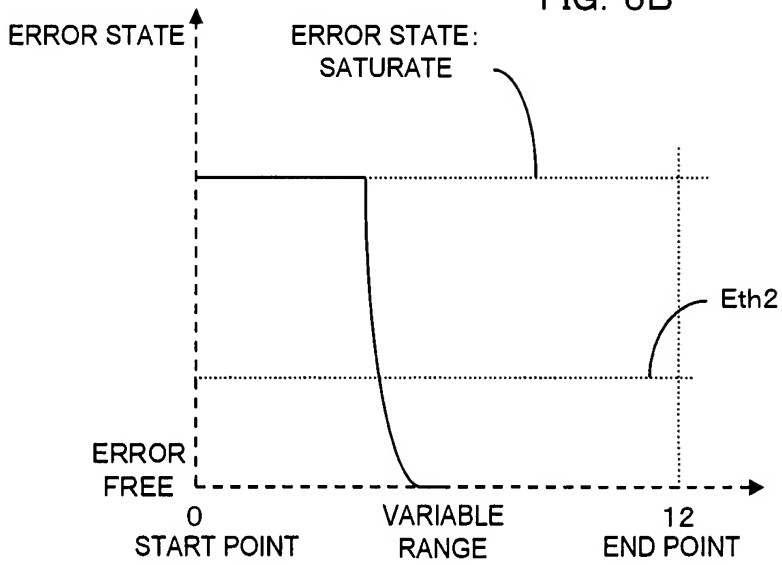



FIG. 6C

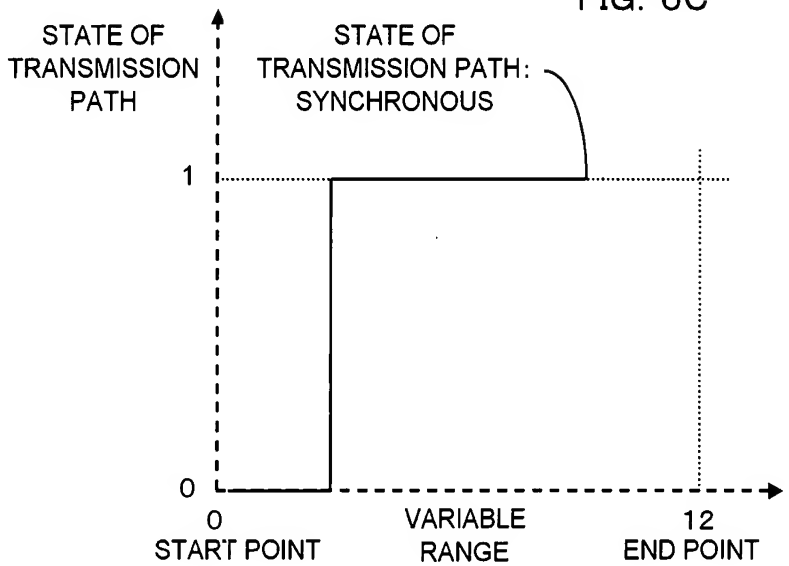



FIG. 6D

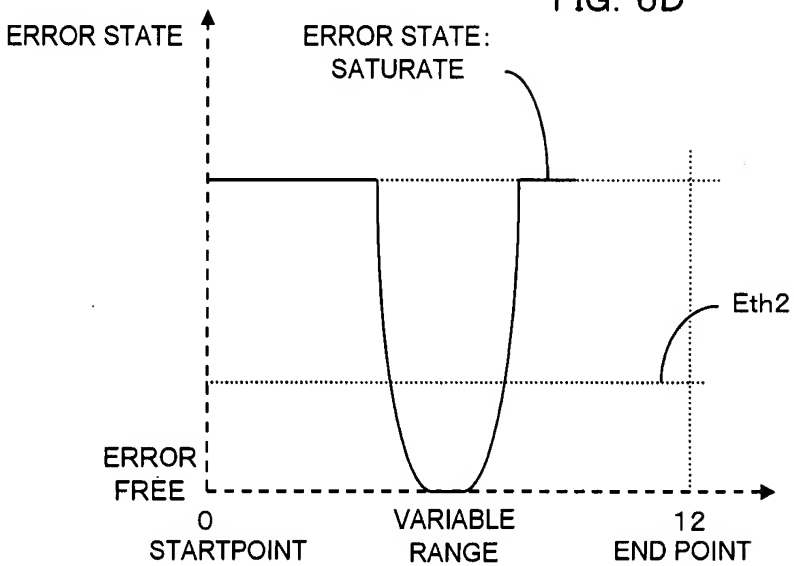


FIG. 7A

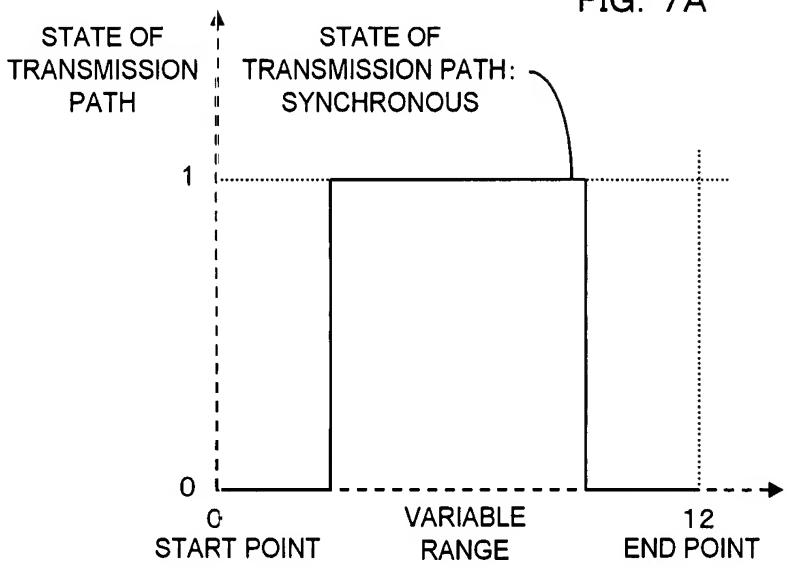

STATE OF TRANSMISSION PATH
STATE OF TRANSMISSION PATH: SYNCHRONOUS
1
0
0
START POINT
VARIABLE RANGE
12
END POINT

FIG. 7B

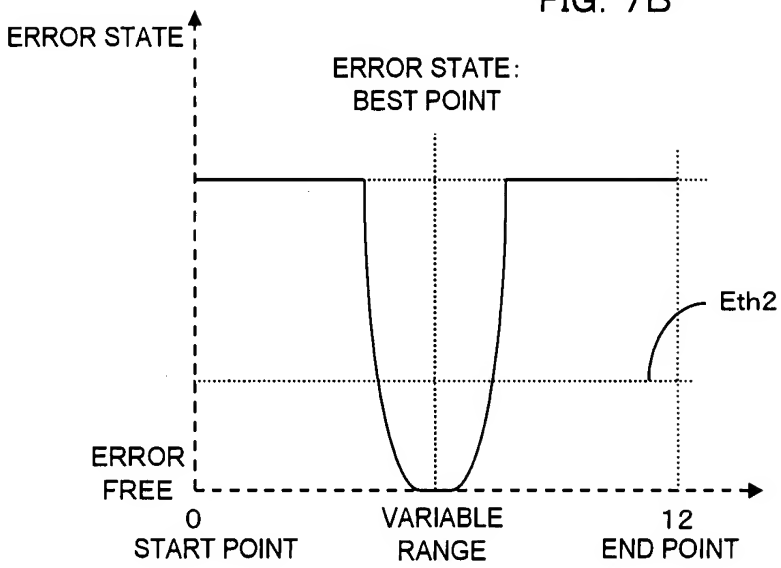

ERROR STATE
ERROR STATE: BEST POINT
Eth2
ERROR FREE
0
START POINT
VARIABLE RANGE
12
END POINT

FIG. 8A

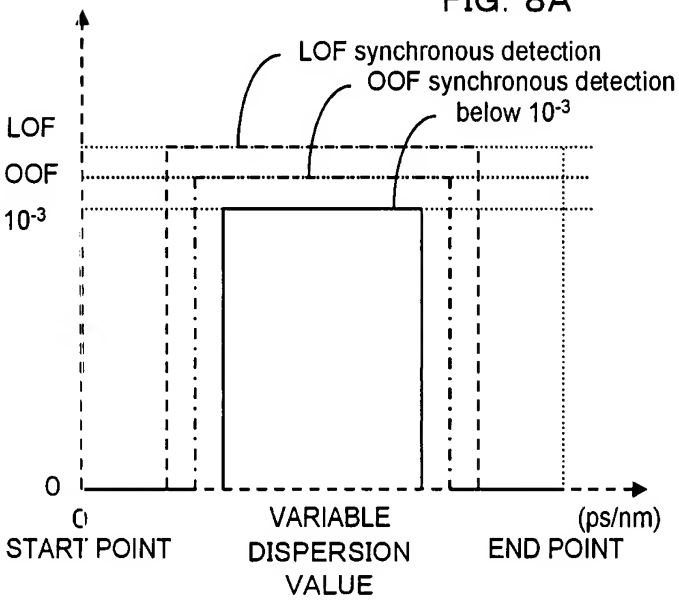



FIG. 8B

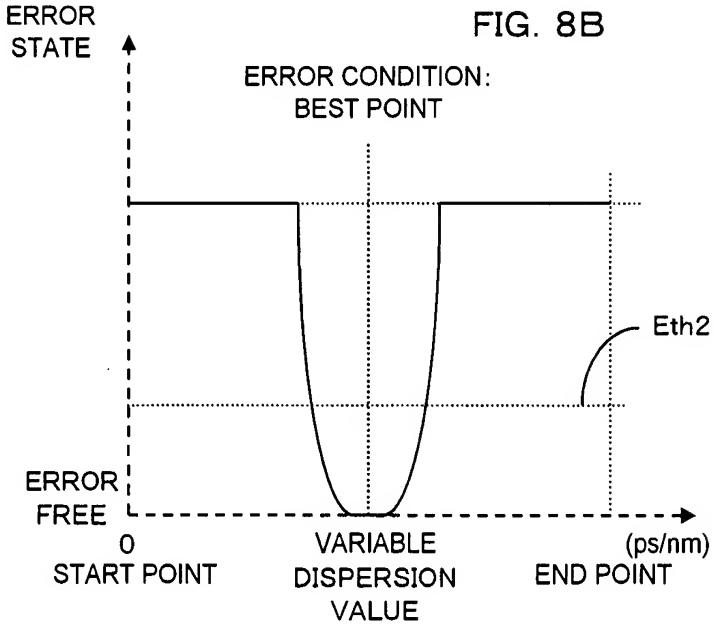



FIG. 8C

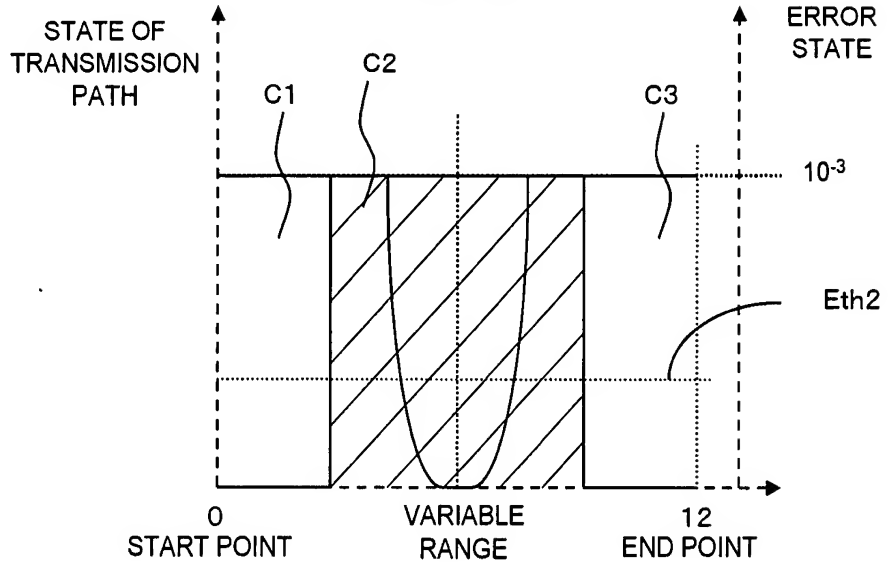


FIG. 9

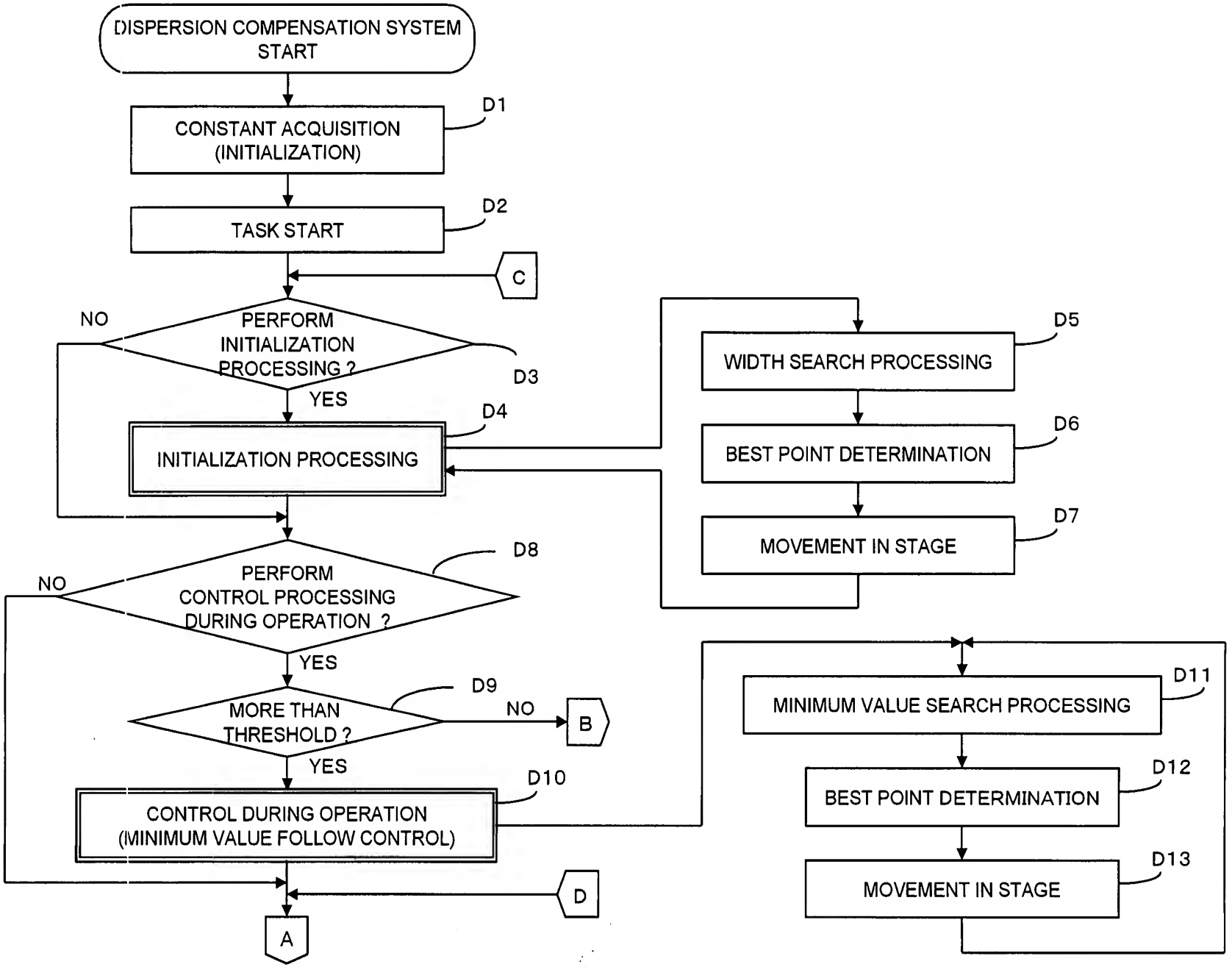
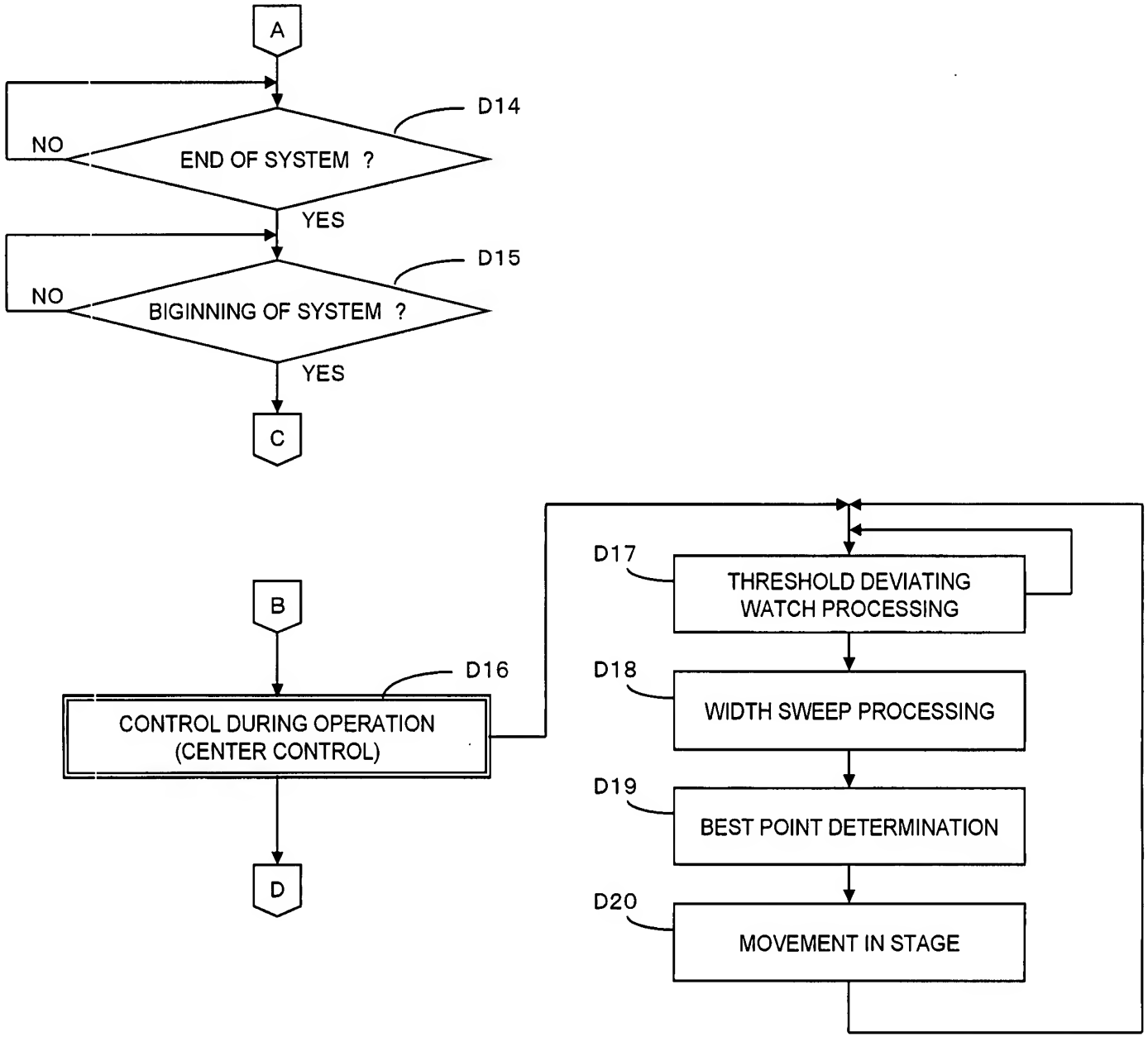

DISPERSION COMPENSATION SYSTEM START
CONSTANT ACQUISITION (INITIALIZATION)
D1
TASK START
D2
C
NO
PERFORM INITIALIZATION PROCESSING ?
D3
YES
INITIALIZATION PROCESSING
D4
WIDTH SEARCH PROCESSING
D5
BEST POINT DETERMINATION
D6
MOVEMENT IN STAGE
D7
NO
PERFORM CONTROL PROCESSING DURING OPERATION ?
D8
YES
MORE THAN THRESHOLD ?
D9
NO
B
YES
CONTROL DURING OPERATION (MINIMUM VALUE FOLLOW CONTROL)
D10
MINIMUM VALUE SEARCH PROCESSING
D11
BEST POINT DETERMINATION
D12
MOVEMENT IN STAGE
D13
D
A

FIG. 10


A
D14
NO
END OF SYSTEM ?
YES
D15
NO
BIGINNING OF SYSTEM ?
YES
C
B
D16
CONTROL DURING OPERATION
(CENTER CONTROL)
D
D17
THRESHOLD DEVIATING
WATCH PROCESSING
D18
WIDTH SWEEP PROCESSING
D19
BEST POINT DETERMINATION
D20
MOVEMENT IN STAGE

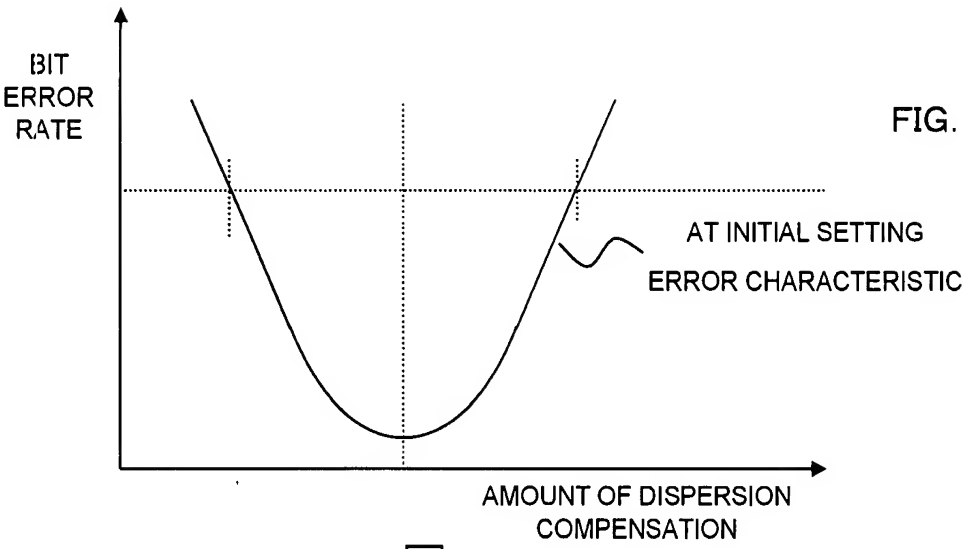



FIG. 11A

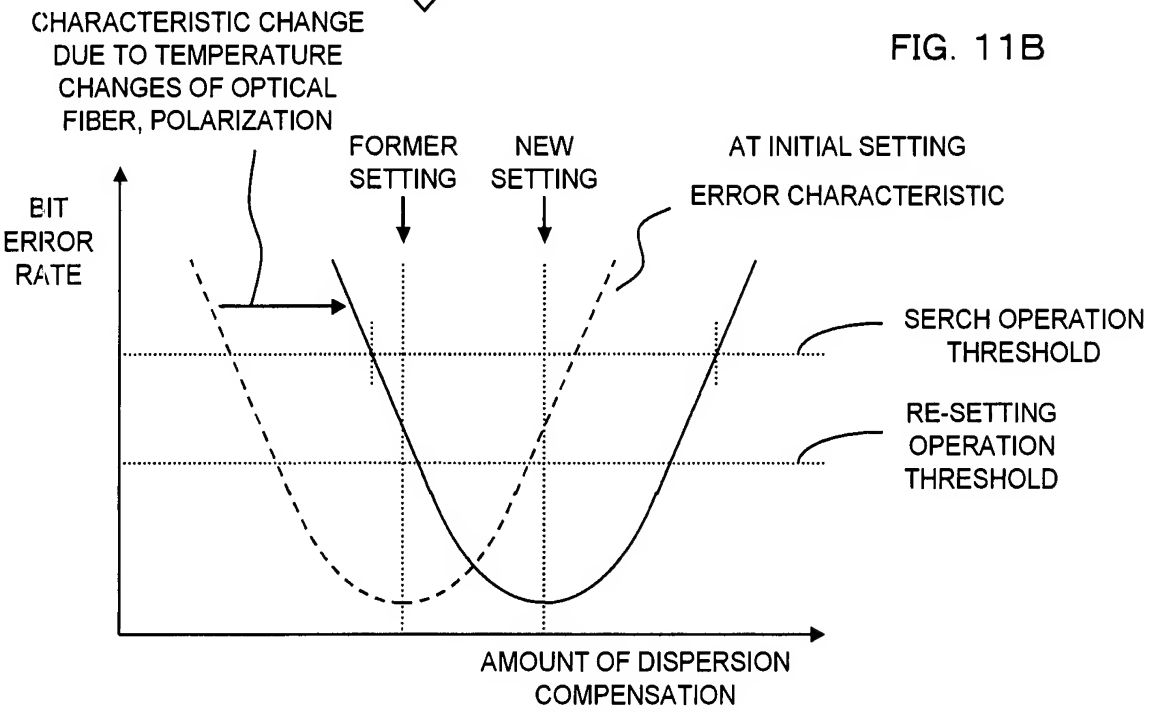



FIG. 11B

FIG. 12A

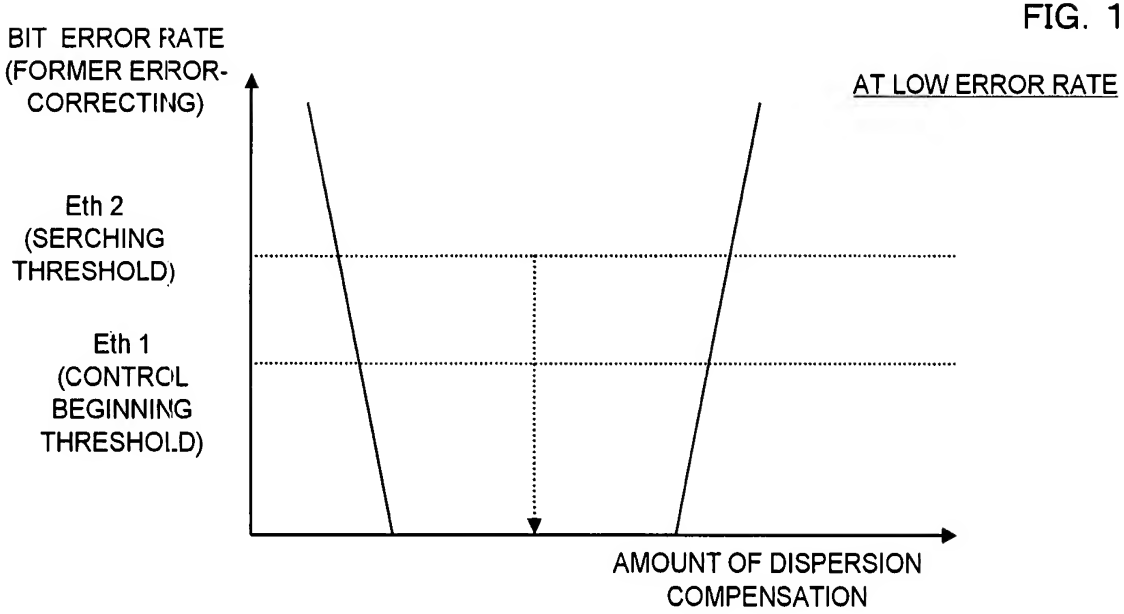



FIG. 12B

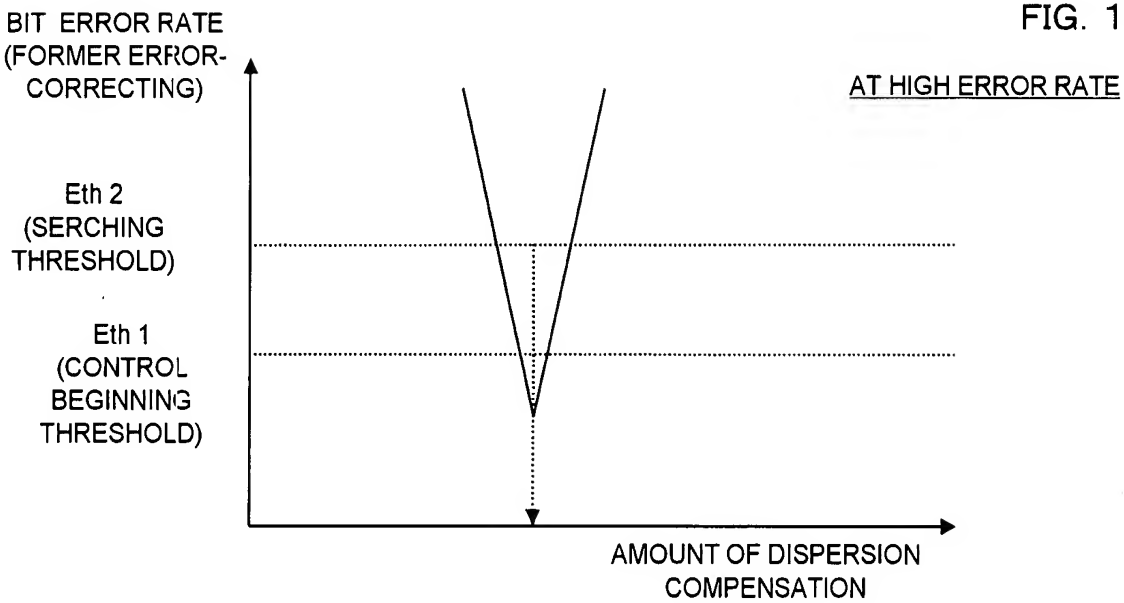


FIG. 13

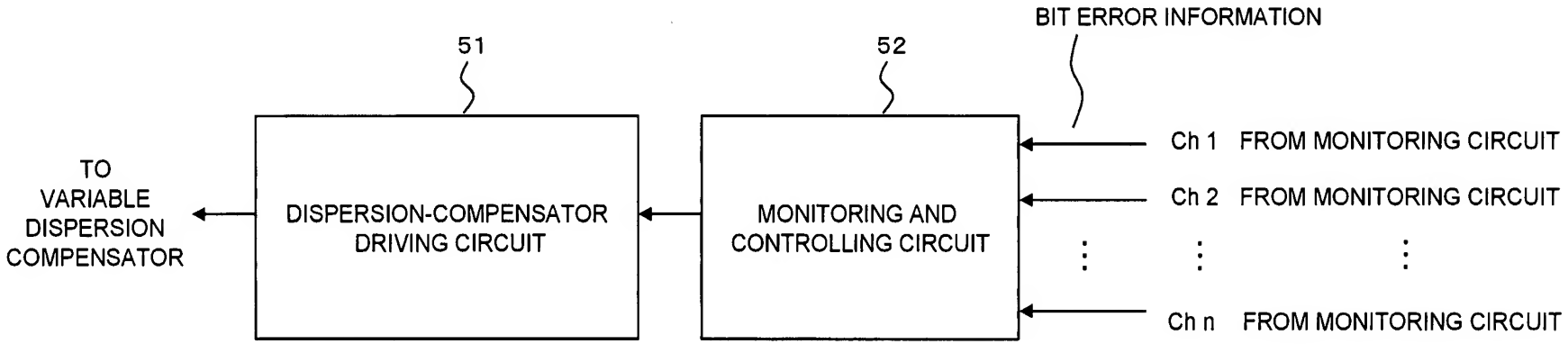

BIT ERROR INFORMATION
51
52
TO VARIABLE DISPERSION COMPENSATOR
DISPERSION-COMPENSATOR DRIVING CIRCUIT
MONITORING AND CONTROLLING CIRCUIT
Ch 1 FROM MONITORING CIRCUIT
Ch 2 FROM MONITORING CIRCUIT
Ch n FROM MONITORING CIRCUIT

FIG. 14

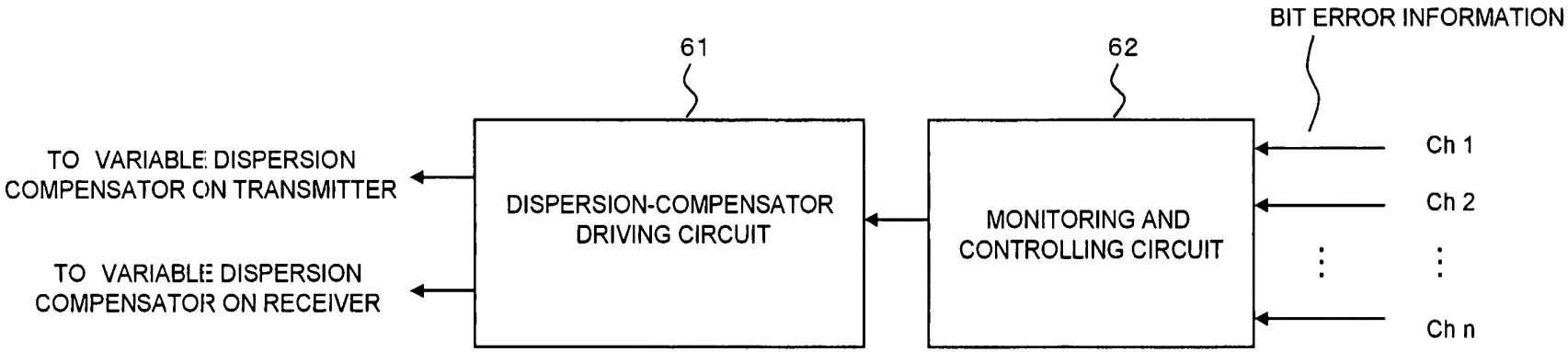

BIT ERROR INFORMATION
61
62
TO VARIABLE DISPERSION COMPENSATOR ON TRANSMITTER
TO VARIABLE DISPERSION COMPENSATOR ON RECEIVER
DISPERSION-COMPENSATOR DRIVING CIRCUIT
MONITORING AND CONTROLLING CIRCUIT
Ch 1
Ch 2
Ch n

FIG. 15

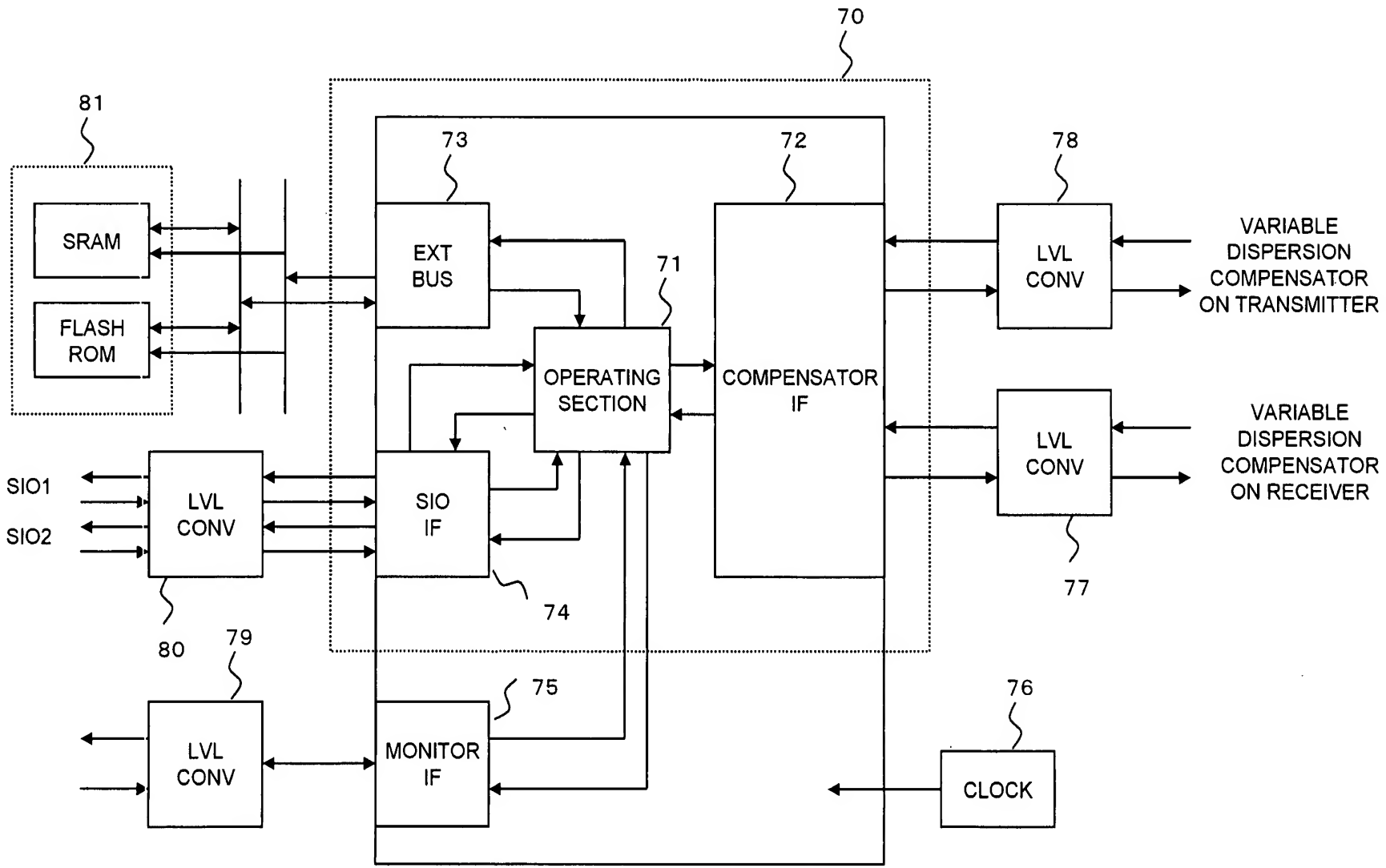

70
81
73
72
78
SRAM
FLASH ROM
EXT BUS
71
OPERATING SECTION
COMPENSATOR IF
LVL CONV
VARIABLE DISPERSION COMPENSATOR ON TRANSMITTER
LVL CONV
VARIABLE DISPERSION COMPENSATOR ON RECEIVER
77
SIO1
SIO2
LVL CONV
SIO IF
74
80
79
75
76
LVL CONV
MONITOR IF
CLOCK

FIG. 16

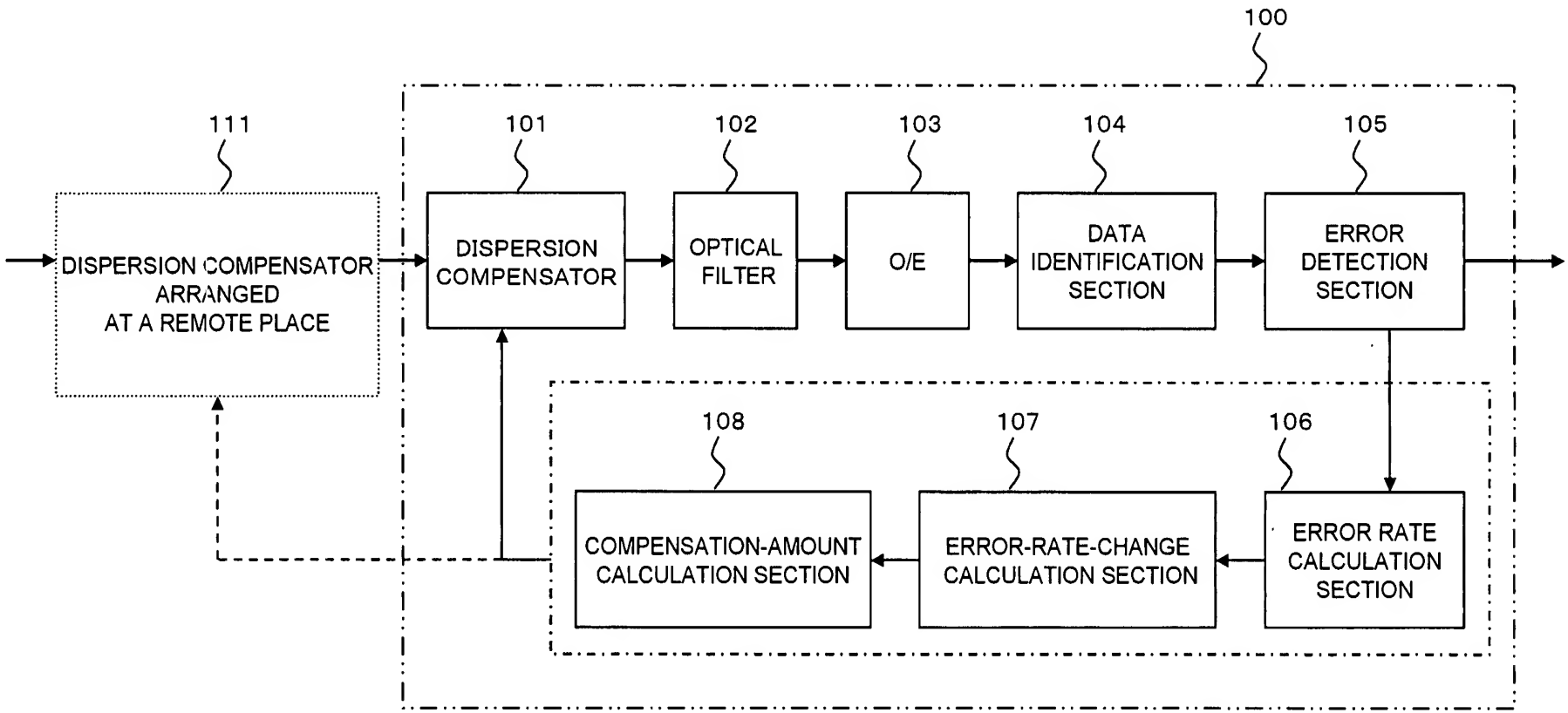
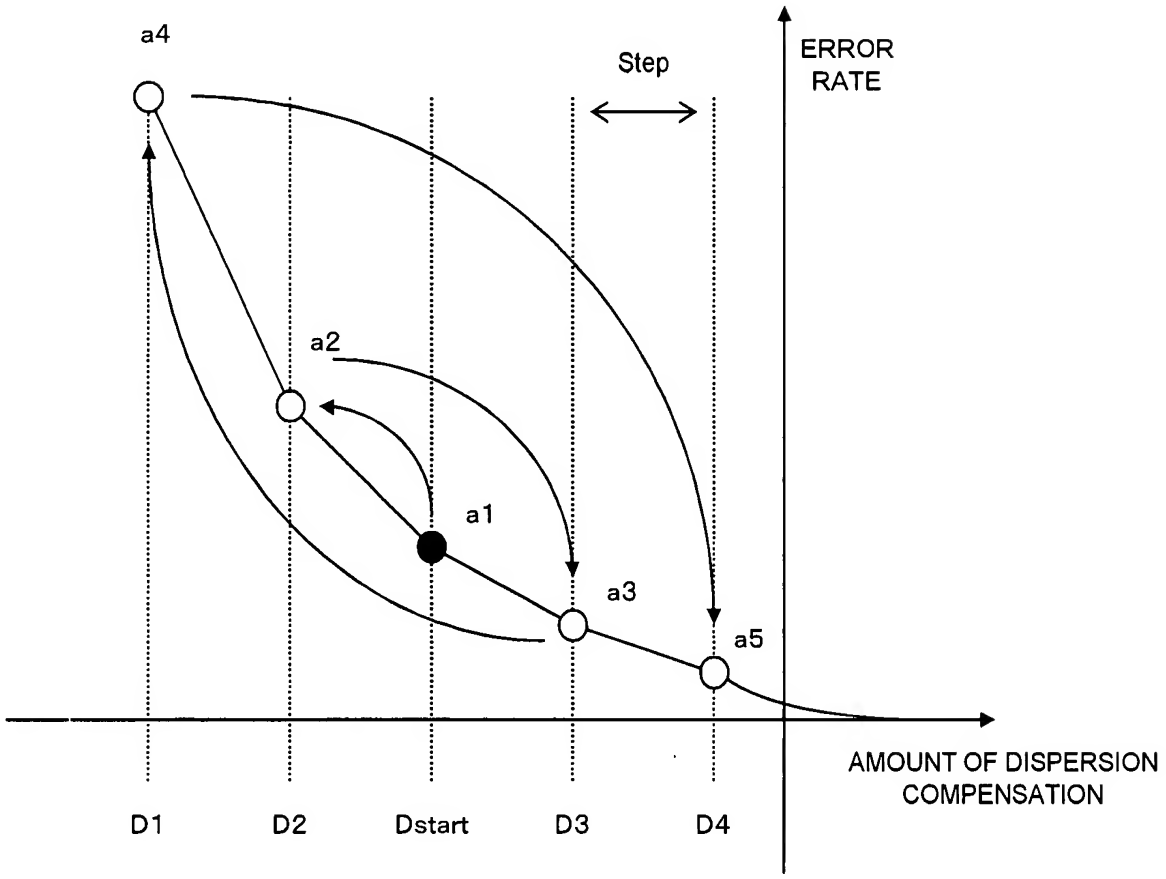

100
111
101
102
103
104
105
DISPERSION COMPENSATOR ARRANGED AT A REMOTE PLACE
DISPERSION COMPENSATOR
OPTICAL FILTER
O/E
DATA IDENTIFICATION SECTION
ERROR DETECTION SECTION
108
107
106
COMPENSATION-AMOUNT CALCULATION SECTION
ERROR-RATE-CHANGE CALCULATION SECTION
ERROR RATE CALCULATION SECTION

FIG. 17


a4
Step
ERROR
RATE
a2
a1
a3
a5
AMOUNT OF DISPERSION
COMPENSATION
D1
D2
Dstart
D3
D4

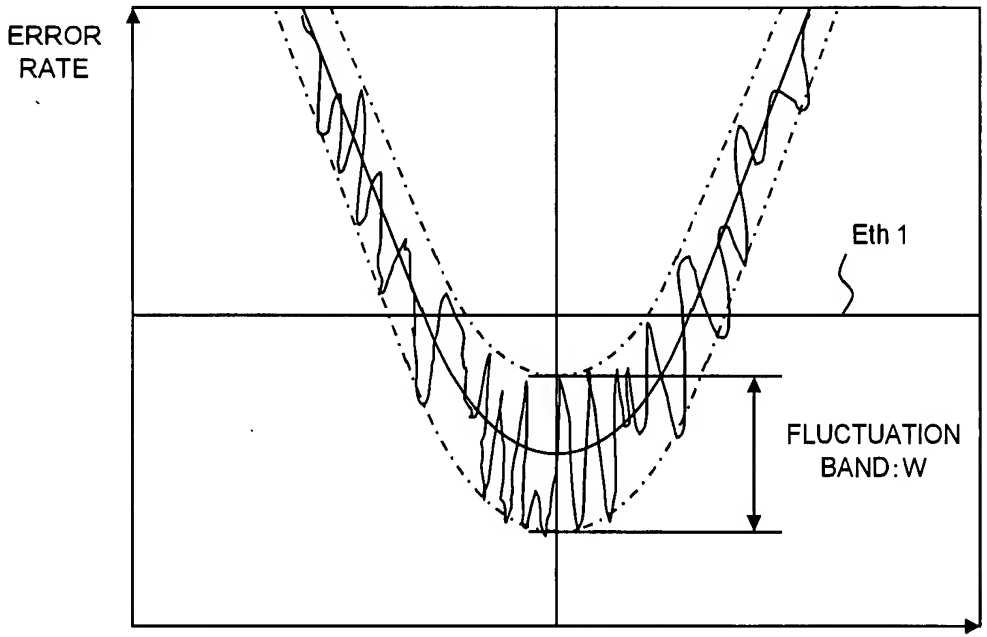



FIG. 18A

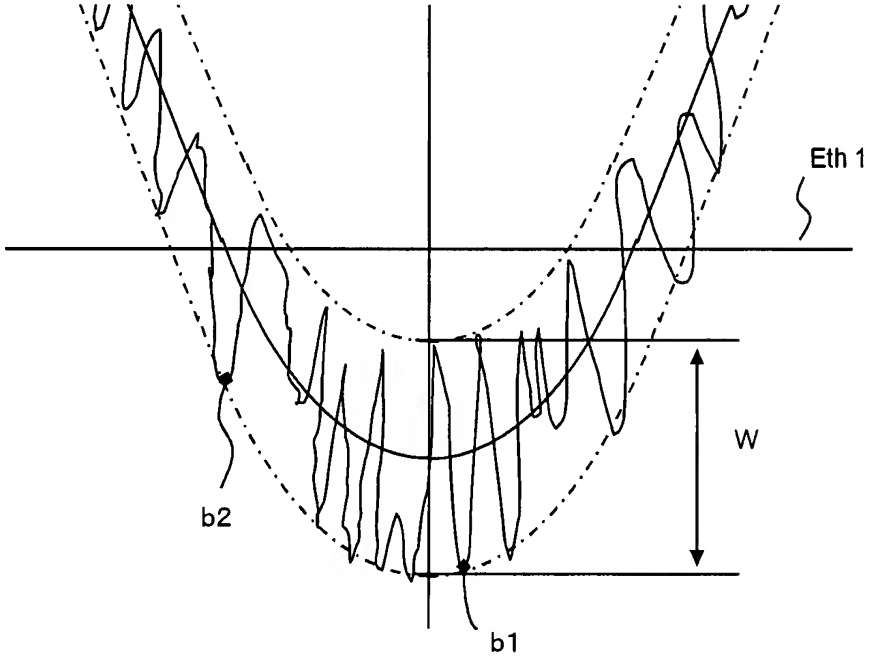



FIG. 18B